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(72) Inventors:
• Zun, Zhiping
Belfast BT8 6XW, Northern Ireland (GB)
• Hu, Yi
Belfast, Northern Ireland (GB)

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(74) Representative: Wallace, Alan
F. R. Kelly & Co.
4 Mount Charles
Belfast BT7 1NZ, Northern Ireland (GB)

(71) Applicant: Amphion Semiconductor Limited
Belfast BT9 5BS (GB)

(54) Accelerator architecture for a speech codec

(57) A codec (110) comprising a programmed digital signal processor (112) and an accelerator core (116) in which computation of a coding algorithm is divided between the digital signal processor (112) and the accel-

erator core (116), computationally relatively intensive parts of a coding algorithm being performed by the accelerator core. In the preferred embodiment, the instruction set is optimised to perform CELP coding of speech signals.

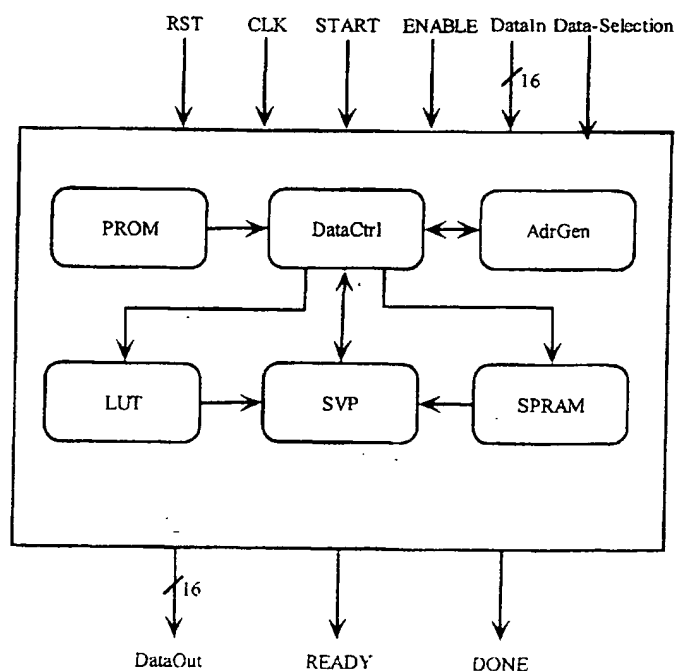


Fig 2

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ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO.

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Application Number

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Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
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The present search report has been drawn up for all claims			
Place of search	Date of completion of the search	Examiner	
MUNICH	3 February 2004	Zimmermann, E	
CATEGORY OF CITED DOCUMENTS			
X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons ----- & : member of the same patent family, corresponding document			

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